Performance Comparison and Overview of Different Approaches for VLSI Optoelectronic Interconnects

Yun-Parn Lee and Yulei Zhang

***Abstract*—Although a great deal of research has been carried out over the last decade in which many different approaches for devising optoelectronic interconnects have been proposed, more detailed analysis of the performance parameters such as power, latency, and area of different optical technologies is yet to be done. Optoelectronics offer potential for new approaches to the production of VLSI interconnects, but previous works have made overly simplified assumptions for optoelectronic interconnections. In this paper, we present a preliminary analysis of the system parameters of different optoelectronic interconnect technologies. Based on our analysis, we conclude that the three-dimensional free-space optoelectronic interconnect network has the best speed area product performance compared with fiber-optical interconnects and optical microelectromechanical systems (MEMS) interconnects. Second, although the optoelectronic interconnect offers higher data rates and less power per bit compared with electronic interconnects, the bipolar encoding scheme on the source plane and the detector plane means that a larger area and volume will be needed.**

***Index Terms*—3-D free-space holographic interconnection network; Optical MEMS interconnect; Truth table; VCSEL; Modulators; Detectors; Optical bus**.

I. Introduction

Optical interconnection research aims to replace the electrical interconnection of electronic devices with optical waves. From physics, we know that electrical interconnection and optical interconnection [1] take advantage of two different types of physical phenomena. Electrical interconnection [2,3] necessitates downscaling the feature size of the transistor. Although this may increase the computation speed, the tighter packaging may also increase the parasitic capacitance and signal propagation delay. In addition, since the electrical interconnection is treated as a uniform RLC transmission line, the coupling capacitance and on-chip self-inductance may lead to additional delay and cross-talk. This means that electronic interconnects are prone to encountering the bottleneck [4] due to computational bandwidth limitations. Also, when the computational bandwidth increases, connection impedance mismatch may become a critical factor.

Li and Popelek [5,6] performed a volume consumption comparison of free-space and guided-wave optical interconnection. They showed that the single micro aperture-per-channel implementations of either space-invariant or space-variant operations are more volume efficient than their two-cascade counterparts and that free-space optics is less volume efficient than guided-wave fiber optics. However, their free-space optical interconnection primarily focuses on point-to-point interconnection. If new methods can be used successfully to convert the combinational circuits used in the electronic interconnect, such that each type of combinational circuit can be replaced with holographic interconnections and minor electronic circuits, the results of the above comparison might be very different.

In addition, many researchers have proposed holographic interconnections for free-space optical interconnection [7–12]. With holographic interconnections the focus is on interconnection capacity, diffraction efficiency, data rates, and power consumption. Although holographic optical interconnection is indeed three dimensional in nature [12], the Fresnel lens or holograms used to interconnect the optical source and detector array are inherently limited by their geometrics. Moreover, the Fresnel lens is less energy and volume efficient than fiber optics or waveguide interconnection [5].

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Chen *et al.* [13] demonstrated the functioning of the high-speed optical data bus, which is equivalent to the VME bus and FutureBus, using a polyimide waveguide as the interlayer dielectric material to form three-dimensional optical clock distribution. Their excellent work primarily focuses on the clock distribution similar to the VLSI system.

In 1987, Lee [14] proposed a truth-table lookup holographic processor. Lee was the first to suggest the idea of using dual optical sources and dual detector arrays in the holographic optoelectronic interconnect network. Lee was also the first to suggest using the detector's summation circuit, the XOR circuit, and comparison circuit in between sources and detectors. Lee's method can convert any type of digital input to generate a digital output signal.

Ozaktas and co-workers [15–19] applied the results of area-volume complexity theory for solid wires to optical communication systems. They concluded that the optically interconnected electronic circuit represents the best alternative given the physical limitations.

In 1992, Krishnamoorthy *et al.* [20] discussed a holographic imaging optoelectronic interconnection that was a slightly modified version of the traditional 4*f* optoelectronic system. The scaling factor in the optical lens can be designed so that the detector arrays are centered on the source arrays. The MIN and MAX circuits [20] are identical to the comparison circuit in Lee's design [14].

Guilfoyle *et al.* [21] proposed a truth-table decomposition calculation method. Drabik [22] published a similar result related to "3-D optoelectronic free-space interconnects."

Cho *et al.* [23] suggest that optical interconnects are superior to electronic interconnects because of their lower attenuation and lower noise. Ozaktas *et al.* [24] conclude that the multifacet free-space architecture can be used to achieve the smallest possible two-dimensional optoelectronic interconnect.

In Section II, we give an overview of optoelectronic interconnects mentioning previous works including the fiber-optical interconnect, polymer waveguide optical interconnect, Fresnel hologram optical interconnect, 3-D free-space optoelectronic interconnect network, and optical microelectromechanical systems (MEMS) interconnect.

In Section III, we perform mathematical analysis of the optoelectronic switching interconnect network based on a digital truth table. In this section, we will also discuss the algorithm for converting the truth table into a format that is suitable for optoelectronic holographic implementation. In addition, we discuss recent progress on microscale holographic systems as well as deriving the power, area, and latency equations for the 3-D free-space optoelectronic interconnect network system. Simulation results will be presented here.

In Section IV, we discuss recent progress using optical MEMS devices in optoelectronic interconnects. We derive system-related equations for optical MEMS interconnects.

In Sections V and VI, we perform parametric parameter comparisons of the area, latency, and power consumption among different optoelectronic interconnect technologies. We also discuss an example of the calculation using VCSEL and p-i-n photodiodes. Finally, a discussion and conclusions are offered in Section VII.

II. Overview of Optoelectronic Interconnects

The physical properties of photons [25,26] are fundamentally different from those of electrons. Photonic interconnects must have source-to-detector and detector-to-source conversion. To construct large-scale digital devices in optics, one needs to implement the appropriate level of read-only memory (ROM) or programmable logic array (PLA). Any attempts to solve this problem at the transistor level or gate level may fail. This important process has been overly simplified in many previous works.

The performance of a multiprocessor system [27] mainly depends on the bus architecture. The bus architecture is highly related to its bus interconnections. Figure 1 shows a system block diagram of a typical multiprocessor system. Since the bus performance is so dependent on the shorter propagation delay and larger bus width, the optoelectronic interconnection can play an important role in system-on-chip multiprocessor design. Figure 2 demonstrates the bus arbiter circuit [28] in a multiprocessor system.

The system's interconnection can be through a fiber-optical interconnect, Fresnel hologram interconnect, 3-D optoelectronic switching network, or 3-D optoelectronic MEMS interconnect.

If the above circuits are connected using a fiber-optical interconnect or Fresnel hologram interconnect, then the programmable read-only memory (PROM) circuit and bus switching interface inside the bus arbiter circuit must still be implemented with VLSI. One end of the bus switching interface is connected to the optical source, and the other end of the global bus is connected to the optical detector.

However, if the above circuits are connected using a 3-D optoelectronic switching network and 3-D optoelectronic MEMS interconnects, then the bus arbiter circuit and bus switching circuit can be replaced with a computer-generated hologram. As a consequence,

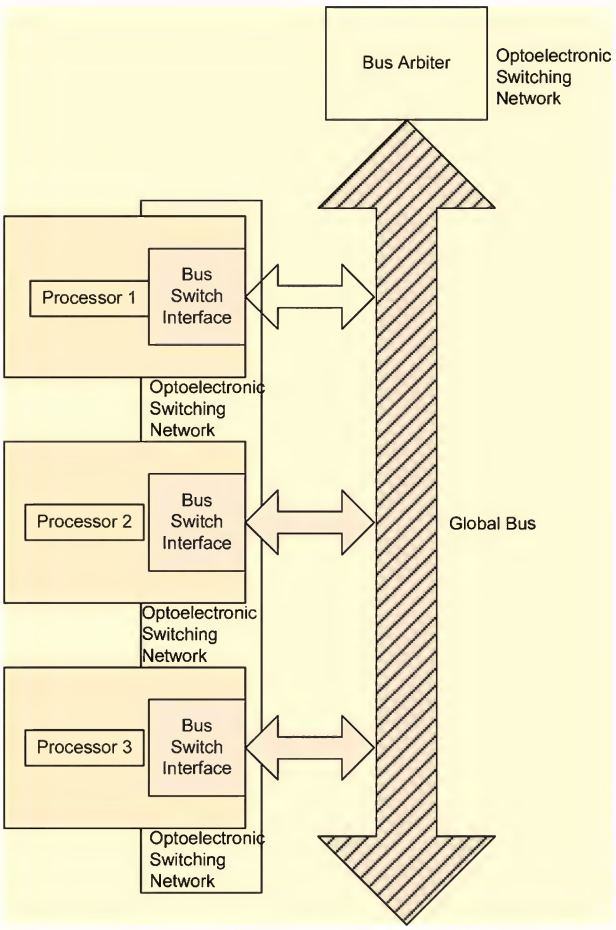

Fig. 1. (Color online) Multiprocessor block diagram.

not only does the switching speed of the system increase, but there also is a larger signal bandwidth and reduction in the total consumed power.

III. Three-Dimensional Free-Space Optoelectronic Switching Network

A. Analysis

Ozaktas and Miller [29] suggested the fundamental optical pipeline principle. Figure 3 shows an outline of the optoelectronic pipeline architecture. For a synchronous digital system, the following relationship must hold:

$$T_{hold} \leqslant T_{comb} \leqslant T - T_{setup}. \tag{1}$$

Thus the time delay T_{comb} is constrained by the system clock period T and hold time T_{hold} [2]. If we want a shorter period or faster speed for the system clock, then we must have a smaller value of T_{comb}. Therefore, if the above combinational logic is implemented in the digital optical system, the value of T_{comb} is approximately equal to

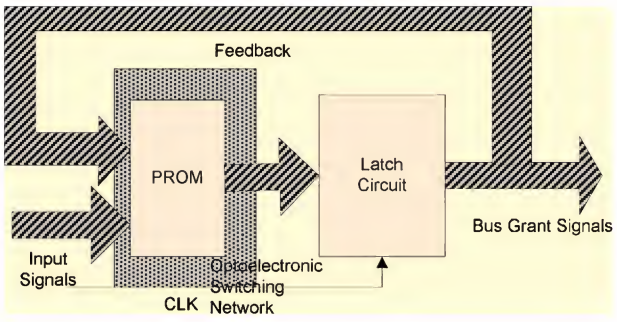

Fig. 2. (Color online) Bus arbiter circuit.

$$T_{comb} \cong N(t_d + t_s). \tag{2}$$

We must have

$$T_{hold} \leqslant N(t_d + t_s) \leqslant T - T_{setup}, \tag{3}$$

where N is the number of stages of conversion between the electronic and optical signal, t_d is the response time of the detector array, and t_s is the response time of the optical source array. Ideally, we would like to see N become as small as possible. We also need to have the smallest values of t_d and t_s.

During the 1970s, computer scientists S. L. Hurst and C. L. Edward studied the use of digital synthesis methods to implement Boolean logic for VLSI designs [30–34]. Their method was later found to work only in certain Boolean functions, and it cannot cover the complete Boolean spectrum. Y.-P. T. Lee [14] and C. C. Lee [35] continued to work on this problem during the 1980s and 1990s. The results are described below.

Definition: Binary Truth Table for Boolean Logic: Boolean logic can be represented by a truth table, a Karnaugh map or a canonical form. A binary truth table with two stable states {0,1} contains m input Boolean variables and n output Boolean functions, and there exist 2^m combinations on a single output Boolean function. We now have a total of $n \times 2^m$ possible outputs. Mathematically, this can be expressed in the following equation:

$$y_k = f_k(x_1, x_2, x_3, \ldots, x_m), \quad k = 1, 2, 3, \ldots, n.$$

Definition: Equivalence of {0,1} and {+1,−1}: The binary {0,1} exclusive or operation is equivalent to the multiplication of {+1,−1}, as shown below:

$\oplus$	1	0
1	0	1
0	1	0

$\times$	−1	+1
−1	+1	−1
+1	−1	+1

Theorem: Boolean Logic Synthesis in the Optical Domain: A binary truth table $f(x)$ with two stable states {0,1} or bipolar encoding $f(z)$ with two stable states {+1,−1} contains m input and n output functions.

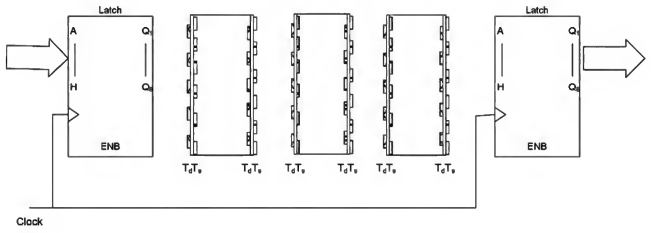

Fig. 3. Optoelectronic pipeline architecture and logic timing constraints.

There exist Boolean basis vectors and Boolean spectral expansion vectors. The inner product of these two vectors is equivalent to the original truth table [14]. The Boolean spectral expansion vector is calculated from the Walsh transform; the Boolean basis vector is generated from the sequence in the corresponding Walsh transform. The mathematical relationship is shown below:

$$[Y] = \sum_{p=0}^{2^m-1} [X_p(x_i)] \otimes [S_p(x_i)], \tag{4}$$

$$[S_p(x_i)] = \frac{1}{2^m}[T^m][Y], \tag{5}$$

$$[Z] = \sum_{p=0}^{2^m-1} [r_p(z_i)] \otimes [R_p(z_i)], \tag{6}$$

$$[R_p(z_i)] = \frac{1}{2^m}[T^m][Z], \tag{7}$$

$$z_i = 1 - 2x_i, \tag{8}$$

where $[T^m]$ is the mth-order discrete Walsh transform and $\otimes$ stands for the inner product. The Walsh transform can be a Walsh–Hadamard transform, Rademacher–Walsh transform, or Walsh–Kaczmarz transform. In Eqs. (4)–(8), x_i are the truth-table Boolean variables obtained using {0,1} coding, z_i are the truth-table Boolean variables obtained using $\{+1,-1\}$ coding, $X_p(x_i)$ represents the Boolean basis vector obtained using {0,1} coding, $r_p(z_i)$ represents the Boolean basis vector obtained using $\{+1,-1\}$ coding, $S_p(x_i)$ represents the spectral expansion vector obtained using {0,1} coding, and $R_p(z_i)$ represents the spectral expansion vector obtained using $\{+1,-1\}$ coding.

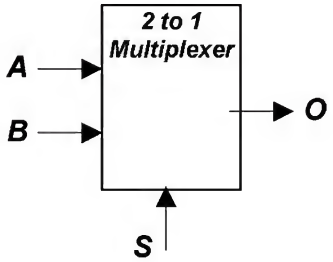

Fig. 4. Two-to-one multiplexer diagram.

(A)X_1	(B)X_2	(S)X_3	f(x)	f(z)
0	0	0	0	+1
0	0	1	0	+1
0	1	0	1	-1
0	1	1	0	+1
1	0	0	0	+1
1	0	1	1	-1
1	1	0	1	-1
1	1	1	1	-1

Fig. 5. Binary truth table for a two-to-one multiplexer diagram.

Three Variable Example: The multiplexer, decoder, and arithmetic circuits are important combinatorial circuits in a digital design. The multiplexer selects one of several input signals to send to a signal output. Figures 4 and 5 show a diagram of a multiplexer and its binary truth table. This multiplexer can be implemented with optoelectronics as follows:

A demultiplexer performs reversed operation of a multiplexer, taking a single input to send to one data output. The multiplexer and decoder are extremely important in any type of bus connection circuits. The three input variable truth tables shown below are chosen as an example of a multiplexer, two-to-four decoders, and a one-to-four demultiplexer circuit in a free-space optoelectronics network. The first column of the Z matrix represents a two-to-one multiplexer, the second to the fifth columns represent a two-to-four decoder, and the unused rows are filled with 0's. The sixth to the eighth columns represent a one-to-four demultiplexer. The calculation of the spectral expansion matrix is shown below:

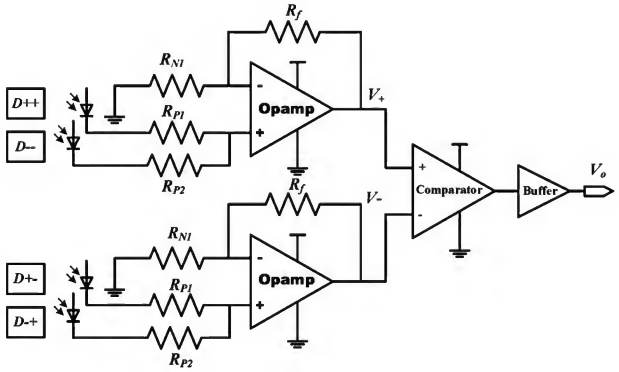

Fig. 6. Detector arrays and comparator.

$$R = TZ = \frac{1}{8}\begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix}\begin{bmatrix} 1 & 1 & 1 & 1 & -1 & 1 & 1 & 1 \\ 1 & 1 & 1 & -1 & 1 & 1 & 1 & -1 \\ -1 & 1 & -1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & 1 & 1 & 1 & -1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ -1 & 1 & 1 & 1 & 1 & -1 & 1 & 1 \\ -1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ -1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

$$= \frac{1}{8}\begin{bmatrix} 0 & 6 & 6 & 6 & 6 & 6 & 6 & 6 \\ 0 & 2 & -2 & 2 & -2 & 2 & 2 & 2 \\ 4 & 2 & 2 & -2 & -2 & -2 & 2 & -2 \\ 4 & -2 & 2 & 2 & -2 & 2 & -2 & 2 \\ 4 & -2 & -2 & -2 & -2 & 2 & -2 & -2 \\ -4 & 2 & -2 & 2 & -2 & -2 & 2 & 2 \\ 0 & 2 & 2 & -2 & -2 & 2 & 2 & -2 \\ 0 & -2 & 2 & 2 & -2 & -2 & -2 & 2 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0.7500 & 0.7500 & 0.7500 & 0.7500 & 0.7500 & 0.7500 & 0.7500 \\ 0 & 0.2500 & -0.2500 & 0.2500 & -0.2500 & 0.2500 & 0.2500 & 0.2500 \\ 0.5000 & 0.2500 & 0.2500 & -0.2500 & -0.2500 & -0.2500 & 0.2500 & -0.2500 \\ 0.5000 & -0.2500 & 0.2500 & 0.2500 & -0.2500 & 0.2500 & -0.2500 & 0.2500 \\ 0.5000 & -0.2500 & -0.2500 & -0.2500 & -0.2500 & 0.2500 & -0.2500 & -0.2500 \\ -0.5000 & 0.2500 & -0.2500 & 0.2500 & -0.2500 & -0.2500 & 0.2500 & 0.2500 \\ 0 & 0.2500 & 0.2500 & -0.2500 & -0.2500 & 0.2500 & 0.2500 & -0.2500 \\ 0 & -0.2500 & 0.2500 & 0.2500 & -0.2500 & -0.2500 & -0.2500 & 0.2500 \end{bmatrix}, \quad (9)$$

where R is the spectral expansion matrix for optoelectronic connection circuits, T is the Walsh–Hadamard transform, and Z is the input Boolean basis vector.

$$r_p(z_i) = \begin{bmatrix} R_0 \\ R_3 \\ R_2 \\ R_2R_3 \\ R_1 \\ R_1R_3 \\ R_1R_2 \\ R_1R_2R_3 \end{bmatrix}, \quad X_P(x_i) = \begin{bmatrix} 1 \\ x_3 \\ x_2 \\ x_2 \oplus x_3 \\ x_1 \\ x_1 \oplus x_3 \\ x_1 \oplus x_2 \\ x_1 \oplus x_2 \oplus x_3 \end{bmatrix}. \quad (10)$$

Figure 6 shows a diagram of detector arrays, a comparator circuit for single-column truth-table output. The inputs of the truth table go through the Boolean operation circuit shown in Figs. 7–9 to form the Boolean basis vector in the optical source arrays.

For Fig. 6, we derive the following equations for the addition of two photodetectors. After properly adjusting the value of R_{P1} and R_{P2}, this circuit can successfully add together the output of the two photodetectors:

$$V_+ = \left(1 + \frac{R_f}{R_{N1}}\right)\left(\frac{R_P}{R_{P1}}V_{D++} + \frac{R_P}{R_{P2}}V_{D--}\right), \quad (11)$$

where

$$R_P = \frac{R_{P1}R_{P2}}{R_{P1} + R_{P2}}. \quad (12)$$

The second part of Fig. 6 shows a comparator. The differential comparator is an amplification circuit that can multiply the difference between two inputs by the differential gain. The output voltage and the common mode rejection ratio (CMRR) of the comparator can be expressed as

$$V_O = A_d(V_+ - V_-) + A_{CM}\left(\frac{V_+ + V_-}{2}\right), \tag{13}$$

$$\text{CMRR} = 20 \log \frac{|A_d|}{|A_{CM}|}, \tag{14}$$

where V_+ and V_- are the two input voltages, V_O is the output voltage, A_d is the differential mode gain, and A_{CM} is the common mode gain. The example shown here only demonstrates three inputs; however, the above example can be extended to a truth table with four or five input variables. In the case of a truth table with five input variables, we may replace the circuit in Fig. 8 with that of Fig. 9. A truth table with 10 inputs ($m = 10$) is equivalent to a 1 K optoelectronic ROM.

Figures 7–9 show the differential cascade voltage switching logic. Using positive feedback to shorten the switching time, we can estimate the switching time as follows [36]:

$$t_{delay} \cong 0.35 R_N C_{OXN} N^2, \tag{15}$$

where t_{delay} is the total time delay in cascade switching logic, N is the number of metal-oxide semiconductor field-effect transistor (MOSFET) gates, and $R_N C_{OXN}$ indicates the process parameters. This is about 2.1 for the 50 nm process. Therefore, for the circuit shown in Fig. 8, the switching time delay is about 6.6 ns.

B. Architecture and Implementation

In this section, we perform system parameters analysis on the 3-D optoelectronic free-space interconnection network.

Optical experimental results for dual sources and dual detectors have already been demonstrated by many laboratories such as the University of California, San Diego (UCSD) [37–39], Stanford University [40,41], Germany [42–45], the University of Arizona [46], and the U.S. Air Force [47,48].

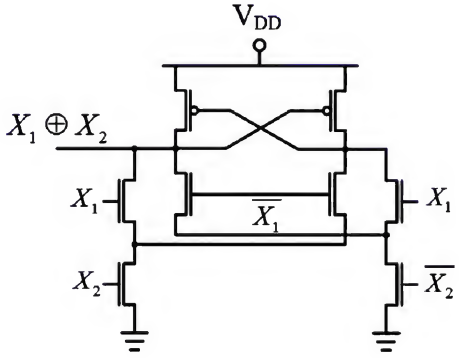

Fig. 7. Circuit to implement a two-variable Boolean basis vector [36].

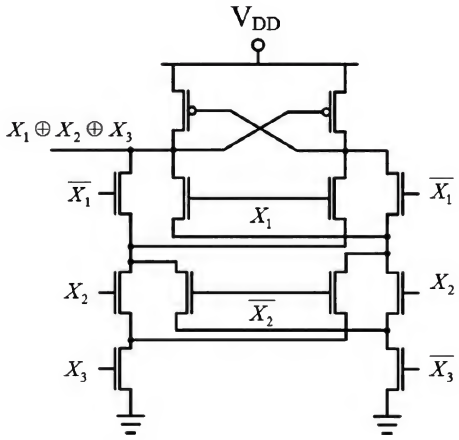

Fig. 8. Circuit to implement a three-variable Boolean basis vector [36].

For a traditional $4f$ optical system, the input plane is amplitude modulated, and the output detector plane is also amplitude (intensity) encoded; therefore, the phase information about the filter plane that arrives on the optical detector plane becomes a noise signal [49]. In addition, the phase detector cannot detect phase simultaneously with the amplitude detector. Consequently, we need to use two separate channels [14,50] to encode the positive and the negative signals into a coherent optical system [14]. This is shown in Fig. 10. Refer to Fig. 11, where each source pixel on the optical input plane can be either made with a VCSEL or a spatial light modulator. Note that the VCSEL is normally made with GaAs, and the XOR gates are made with the complementary metal-oxide semiconductor (CMOS) process. This means that two different types of material must be used in the flip chip bonding process to combine the two.

Referring to Fig. 12, the positive pair on the input plane is indicated with two positive signs and the

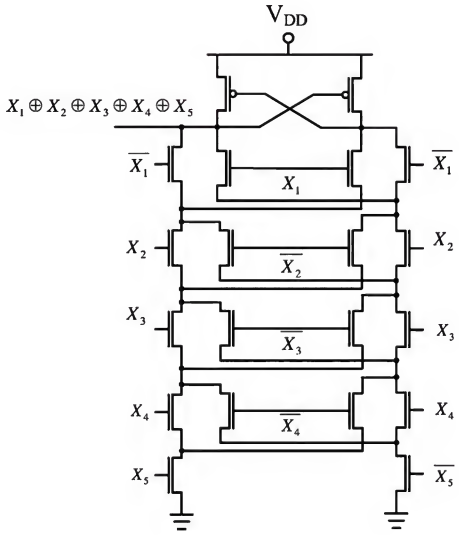

Fig. 9. Circuit to implement a five-variable Boolean basis vector.

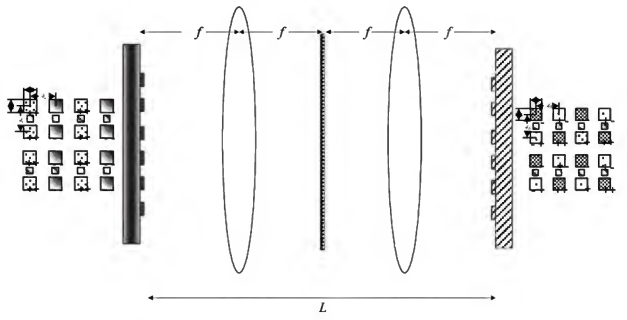

Fig. 10. Traditional free-space optoelectronic interconnection.

negative pair with two negative signs. It is assumed that the combinatorial logic has m inputs and n outputs and a total number of N of the connection logics running in parallel, so one column will need 2^{m+1} pixels in the source array. A total of N columns will need $N \times 2^{m+1}$ pixels in the source array.

According to the Rayleigh criterion [6], for any image-forming optoelectronic system, the minimum resolvable distance is related to the operating wavelength λ, the focus length f, and the lens diameter D by the following equation:

$$d_s = \frac{2.44\lambda f}{D}. \tag{16}$$

According to Fig. 12, assuming the length of each pixel is W_s, the distance between each pixel is d_s, and A_{XOR} for all XOR gates in the source array, then the total area occupied by the source array is

$$A_s = [W_s + (2^{m+1} - 1)d_s][W_s + (2N - 1)d_s] + A_{XOR}N. \tag{17}$$

Apply the same principle to the detector plane as shown in Fig. 13. Note that the positive pair and the negative pair are pointing in opposite directions due to the spatial position exchange of the optical inner product. In addition, we need to include the space

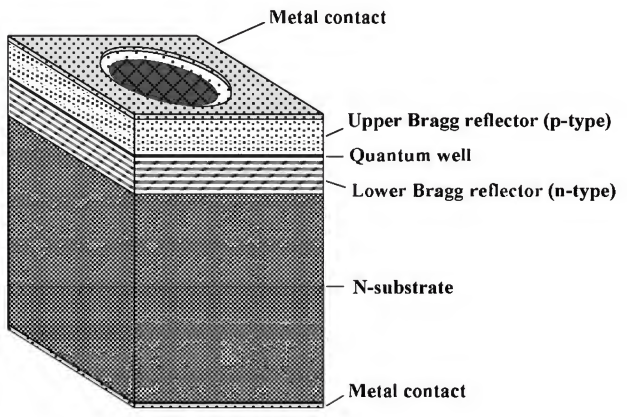

Fig. 11. Input plane—sources, polymer waveguide clock, and the latch.

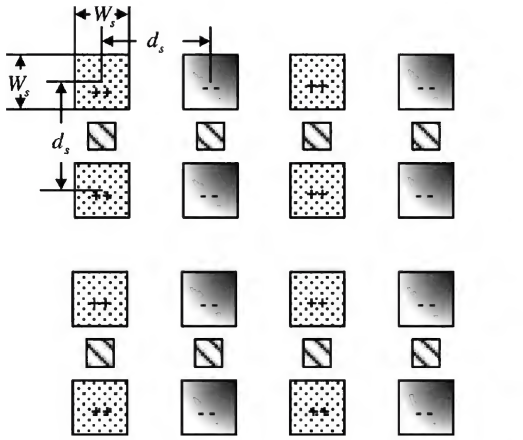

Fig. 12. Optical input array plane, normally constructed with VCSEL arrays with XOR gates and CMOS driver circuits [14].

A_{adders} for the adders and A_{cmps} for the comparators on the detector plane; therefore, we derive the following equations:

$$d_D = \frac{2.44\lambda f}{D}, \tag{18}$$

$$A_D = [W_D + (2n - 1)d_D][W_D + (2N - 1)d_D] + (A_{cmps} + A_{adders}) \times nN. \tag{19}$$

The total occupied area of switching interconnect logics is

$$A_{3D} = A_s + A_D. \tag{20}$$

The total volume is approximately equal to

$$V_{3D} = \frac{1}{2}(A_S + A_D) \times 4f. \tag{21}$$

To calculate the total power consumed by the system, assume each pixel of the VCSEL power is P_S, and each

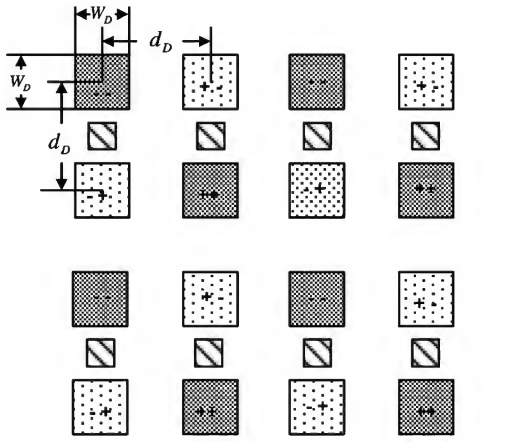

Fig. 13. Optical detector plane, normally constructed with photodector arrays and additional logic circuits [14].

pixel of the detector is P_D. The total consumed power is

$$P_{3D} = 2^{m+2}NP_S + nN \times 4P_d + P_{XOR} + P_{cmps} + P_{adders} \approx (2^{m+2}P_S + 4nP_d) \times N. \quad (22)$$

The total latency delay from the source plane to the next plane is close to

$$t_{3D} = t_s + t_D + t_{XOR} + t_{cmps} + t_{adders}. \quad (23)$$

The traditional optoelectronic system can be shrunk into a much smaller size as shown in Fig. 14. This microscale 3-D free-space interconnect consists of reflective mirror layers, two Fourier transform holograms, and one connection matrix computer-generated hologram (CGH). The distance between the Fourier transform hologram and connection matrix CGH is d. This distance is the same as to the second Fourier transform hologram. The Fourier transform holographic lenses can be obtained through either optimized CGH [51] or recursive design techniques [52]. With the help of a computer-generated hologram [53], the connection matrix R in Eq. (10) is stored in the CGH. There are three types of computer-generated hologram encoding: Lohnmann's method, Lee's method, and Burch's method [53]. The hologram is recorded directly onto the film with a microdensitometer. More recently, an e-beam has been used to perform the same task with greater precision.

In the above analysis of a 3-D free-space optoelectronic interconnect network, the switching logic signals are generated electronically. This makes the encoding bit pattern more accurate and may reduce the bit error propagation.

C. Simulation Results

As shown in Fig. 6, the receiver circuits for the proposed optical interconnection network are composed of two parts, one for the positive signal and one for the negative signal. The received light is first converted into electrical signals by the detector arrays and then added together by the two adders. Next, the results obtained from the two adders are compared using a high-speed analog comparator to generate the truth-table output. The design of the adder and comparator will be discussed in greater detail below. Finally, we summarize the performance of these electronic circuits based on the simulation results using a predictive 45 nm CMOS process.

We use a simple but effective CMOS two-stage op-amp configuration to implement the adder. The structure of this op-amp is shown in Fig. 15. This structure is appropriate for use in high-speed optical signal receivers due to their low noise, stability, and high bandwidth. In this design, we use PMOS as input transistors to reduce the noise; we also adopt a nulling resistance compensation approach to satisfy the stability requirement in the closed-loop application. Furthermore, the phase margin (PM) is made insensitive to process and environment variations by using M9, M10, and M11 transistors to implement the nulling resistor.

The most important design specification of this op-amp is the gain–bandwidth product (GBW). Since the op-amp is used in the closed-loop adder and the bandwidth of present-day photodetectors is normally larger than 10 GHz, we set the GBW specifications to be larger than 10 GHz in this design. Small signal analysis provides the GBW expression shown below:

$$\mathrm{GBW} = g_{m1}/C_C, \quad (24)$$

where g_{m1} is the transconductance of transistor M1 and C_C is the Miller compensation capacitance. The phase margin of this op-amp is given by

$$\mathrm{PM} = 90^\circ - \arctan\left(\frac{g_{m1}}{g_{m3}}\frac{C_L}{C_C}\right) + \arctan\left[\frac{g_{m1}}{g_{m3}}\left(\frac{(W/L)_3}{(W/L)_{11}}\frac{\sqrt{(W/L)_9}}{\sqrt{(W/L)_{10}}} - 1\right)\right], \quad (25)$$

where g_{m3} is the transconductance of transistor M3, C_L is the load capacitance, and $(W/L)_i$ is the size ratio of transistor M_i. Following these two equations, we

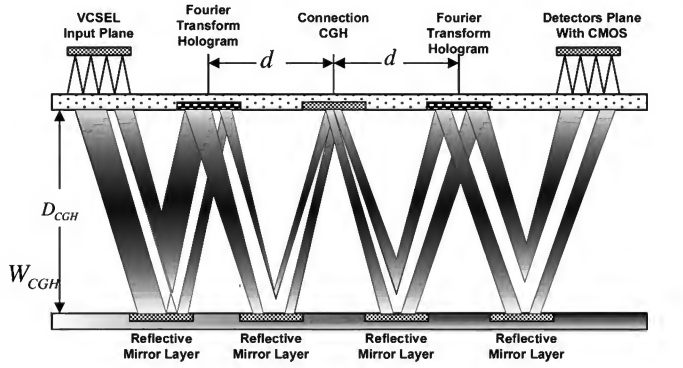

Fig. 14. Microscale 3-D free-space holographic interconnection network.

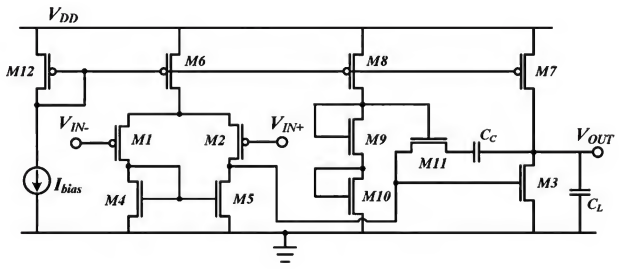

Fig. 15. Structure of the CMOS two-stage op-amp with nulling resistance compensation.

design the op-amp using the 45 nm process, with the assumptions that C_L is 20 fF and the PM should be larger than 50°.

The op-amp structure is simulated in Hspice and some typical results are shown below. The op-amp open-loop frequency response is shown in Fig. 16. We can see that the DC gain of this op-amp is about 42 and the GBW is 10.2 GHz. To verify the insensitivity of the phase margin, we simulate the op-amp open-loop characteristics under three different temperatures. The results show that the PM is maintained in the range of 47°–50°. To verify the functionality and measure the performance data, we perform a closed-loop transient simulation like that shown in Fig. 17. The op-amp is connected with resistors as shown in Fig. 6 to form a small signal adder, and two 10 GHz pulse signals with different amplitudes (50 and 100 mV_{pp}) are added at the inputs. In the simulation, we measure the delay of this adder from the input peak value to the output peak value to be around 90 ps; the power dissipation in this scenario is 260 μW.

The high-speed comparator is implemented using the structure shown in Fig. 18. This structure cascades through several stages to achieve high-speed comparison. The first stage is a differential pair with diode-type loads designed to provide low gain but high bandwidth. In the second stage the positive feedback technique is adopted to amplify the signal difference with higher speed. The signal will be amplified again by a self-biased differential amplifier in the third stage and finally will become a full-swing digital signal buffered by an inverter. Still, the bandwidth of the comparator should be larger than 10 GHz as discussed for the op-amp. During designing, we need to tune the first stage to achieve a high bandwidth with lower but reasonable gain.

The designed comparator circuit is also simulated with Hspice using the same 45 nm process model. Figure 19 shows the DC transfer characteristics of this comparator. From the figure, we can see that the comparator has a DC voltage gain of about 90, corresponding to a 10 mV resolution voltage, and the offset voltage is about 5 mV. A transient simulation is also performed to verify that the circuit is functional at a speed of 10 GHz. The delay of the comparator is 44 ps for a 50 mV input and 58 ps at 10 mV input. The corresponding power dissipation is 470 and 520 μW, respectively.

Finally, we put all the components together and perform an overall simulation to demonstrate the functionality of the receiver system and also measure the performance data. The verification experiment is performed by adding four pulse inputs with different amplitudes (25, 50, 75, and 100 mV) and different pseudorandom binary sequence (PRBS) patterns. The cycle time of the signals is 100 ps (10 GHz). The output of the system with this type of random input is shown in Fig. 20. We can see that the output waveform correctly tracks the difference in the two adders' outputs. Although the delay and power dissipation of this system is data dependent, we measure some different points to find typical values. The delay is around 50 ps, with 53 ps for the rise delay and 47 ps for the fall delay, whereas the power dissipation is about 955 μW including the two op-amps and one compara-

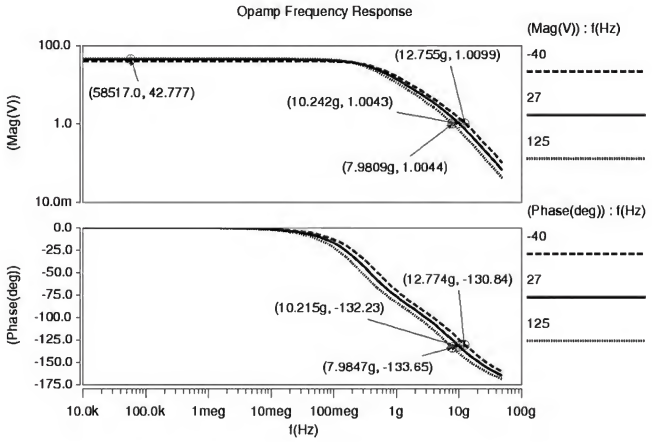

Fig. 16. Open-loop frequency response of the designed op-amp.

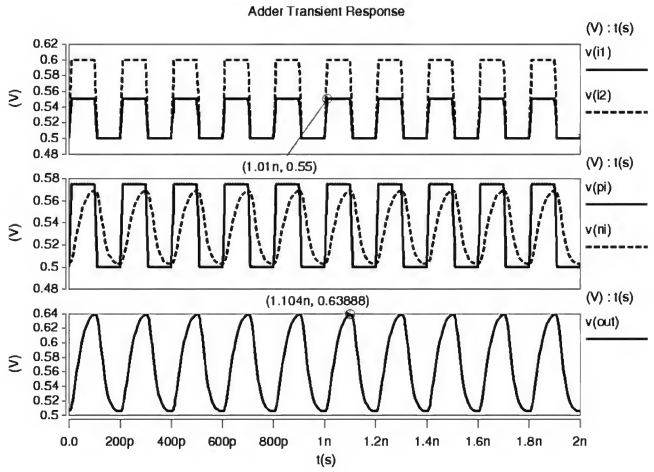

Fig. 17. Closed-loop transient response of the designed op-amp.

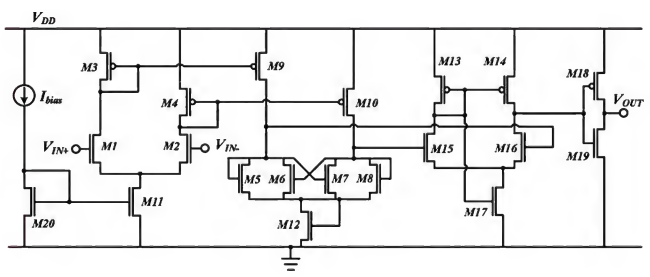

Fig. 18. Structure of the CMOS high-speed comparator with buffered output.

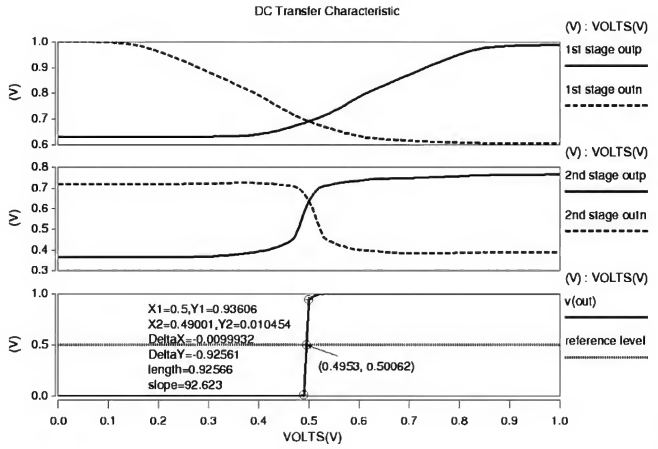

Fig. 19. DC transfer characteristics of the designed comparator.

tor. We can also estimate the total chip area occupied by this electronic receiver. In our design, the two op-amps and one comparator cost $2\times0.15\ \mu m^2 + 0.61\ \mu m^2 = 0.9\ \mu m^2$.

IV. Three-Dimensional Optoelectronic MEMS Interconnect Analysis

In this section, we perform system parameter analysis of the optoelectronic MEMS interconnection system.

invented the world's first MEMS, the deformable mirror device (DMD). Lin and Feldman [54] proposed using DMDs and CGHs to make an optical MEMS interconnect system. Their system diagram is illustrated in Fig. 21. In the figure, arrays of micromachined deformable mirrors are arranged on a silicon substrate.

The optical source in this diagram can be the VCSEL. The optical source sends a light beam vertically to the CGH. The CGH diffracts a total of six beams of light onto two DMDs and four optical detectors on the

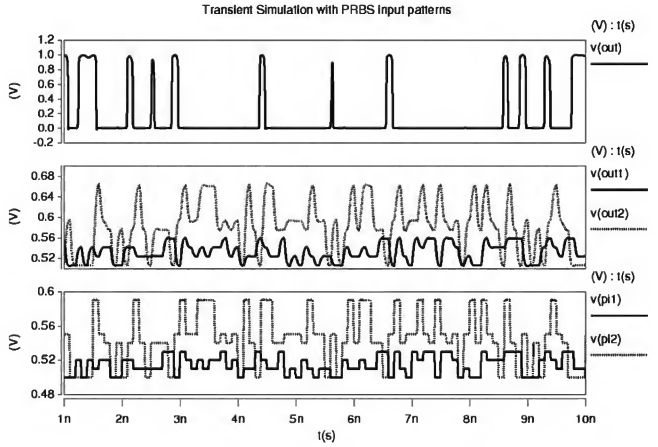

Fig. 20. Overall receiver transient simulation.

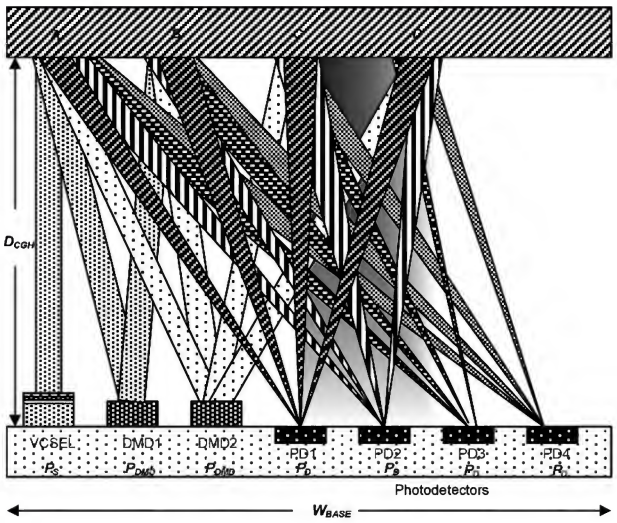

Fig. 21. Optoelectronic MEMS interconnect diagram.

substrate. The beams are again reflected from the DMDs back to the second spot B on the CGH, so that the CGH diffracts four light beams onto four detectors PD1, PD2, PD3, and PD4. If the diffracted light beam is on the same diffraction order, then there is no phase change; otherwise, there is a 180 deg phase change between the first and the second diffraction order among the reflected beams.

Since the DMD is a phase modulator, let the phase of the optical source be ϕ_0. Then the phase at B is $\phi_0+\phi_1$, the phase at C is $\phi_0+\phi_1+\phi_2$, and the phase at D is $\phi_0+\phi_2$, where ϕ_1 and ϕ_2 are the phase shift of the first and the second DMDs. Assume that DMD1 is turned off, then the photodetector PD1 receives a constructive light beam, PD2 receives a destructive light beam, PD3 receives a constructive light beam, and PD4 receives a destructive light beam. Assuming that DMD1 is turned on, the DMD1 modulates the phase by 180 deg. In this case photodetector PD1 receives a destructive light beam, PD2 receives a constructive light beam, PD3 receives a destructive light beam, and PD4 receives a constructive light beam. From each point A, B, C, and D on the CGH, each input light beam is further divided into four beams, and each one will focus on the photodetectors PD1, PD2, PD3, and PD4. If we use +1 to represent an in-phase beam at the photodetector and −1 to represent the 180 deg out-of-phase beam at the photodetector, then we can construct a truth table of interconnection patterns as in Table I. If all four photodetectors are in phase with the optical source, this means that the connection is in the "on" state, otherwise, if only two photodetectors are in phase, then the other two photodetectors are 180 deg out of phase with the optical source, and this means that the connection is in the "off" state.

The movable portion in the MEMS interconnection system uses the spring structure. The fixture beam

TABLE I
TWO INPUT VARIABLES SHOWING THE TRUTH-TABLE INTERCONNECTION PATTERN FOR THE DMD-CGH OPTICAL MEMS INTERCONNECTION SYSTEM

DMD1 State	DMD2 State	PD1				PD2				PD3				PD4			
		A	B	C	D	A	B	C	D	A	B	C	D				
0	0	+1	+1	+1	+1	+1	−1	−1	+1	+1	+1	−1	−1	+1	−1	+1	−1
OFF	OFF		ON				OFF				OFF				OFF		
1	0	+1	−1	−1	+1	+1	+1	+1	+1	+1	−1	+1	−1	+1	+1	−1	−1
ON	OFF		OFF				ON				OFF				OFF		
0	1	+1	+1	−1	−1	+1	−1	+1	−1	+1	+1	+1	+1	+1	−1	−1	+1
OFF	ON		OFF				OFF				ON				OFF		
1	1	+1	−1	+1	−1	+1	+1	−1	−1	+1	−1	−1	+1	+1	+1	+1	+1
ON	ON		OFF				OFF				OFF				ON		

DMD is a MEMS device with four cantilever hinges at right angles. The fixture beam DMD primarily performs phase modulation of light. The three-dimensional DMD structure is shown in Fig. 22. The DMD device has flexure hinges at each end. One end attaches to the support structure, and the other end is attached to the phase plate. This principle is the same as the electric current reflector; both fixed sided beams are distorted and rotated along the direction of the hinges. Since MEMS can produce periodical mechanical oscillations, the periodical oscillation frequency is called the resonant frequency. The resonant frequency of the DMD with the flexure hinges on each end can be expressed as

$$f_o = \frac{D^2 h}{2\pi L^2}\sqrt{\frac{E}{12\rho}}. \tag{26}$$

Therefore, the response time of the DMD can be approximated by the inversion of Eq. (26):

$$t_{DMD} = \frac{2\pi L^2}{D^2 h}\sqrt{\frac{12\rho}{E}}, \tag{27}$$

where D is a constant, normally, $D = 0.48$ at the lowest resonant frequency; E is the elasticity coefficient; L and h are the hinge's length and thickness, respectively; and ρ is the material's density. According to Lin [54,55], actual measurement of the DMD's response time indicates a rise time of 3.5 μs and a fall time of 2.5 μs at 180 deg of phase modulation.

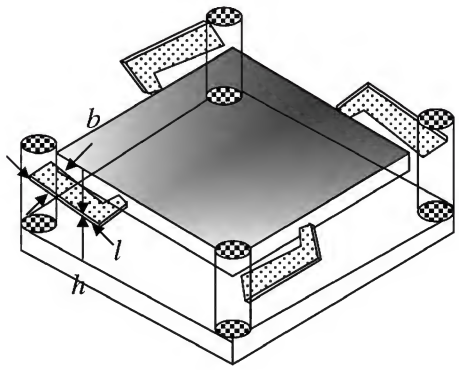

Fig. 22. DMD single-cell diagram.

In general, if we set up the same interconnection l columns on the silicon substrate, for a two input variable truth-table optical MEMS interconnection, the total required power can be expressed as

$$P = (P_S + 2P_{DMD} + 4P_D)l. \tag{28}$$

The optical MEMS interconnection occupies an area of

$$W_{base} = A_s + 4A_D + 2A_{DMD} + 6d, \tag{29}$$

$$A_{MEM} = W_{base}l, \tag{30}$$

where d is the space between the detector and the DMDs or the source and the detector. The total latency delay of the optoelectronic MEMS interconnect is

$$t = t_s + t_D + 2t_{DMD}. \tag{31}$$

In our analysis, note that the truth-table outputs of optical MEMS interconnects are generated optically. Also, the above example only contains two inputs. When the number of input lines increase to three or four, more reflective surfaces and DMDs are involved, which increases the possibility of bit error propagation in the optical data path.

V. LATENCY, AREA, AND VOLUME COMPARISON

In summary, we arrive at the following conclusions in this section. Previously, Li [5,6] did important work analyzing fiber-optical interconnects. There has also been much work done on Fresnel holographic interconnects.

Assume that there are N_C interconnect points, then the area occupied by the fiber-optical interconnect is

$$A_{OF} = N_C(A_S + A_D) + A_{electronic}, \quad (32)$$

where A_S is the area occupied by a source, A_D is the area occupied by a detector, and $A_{electronic}$ is the area of all electronic components. Therefore, the total latency delay is

$$t_{OF} = t_S + t_D + t_{electronic}. \quad (33)$$

The physical principle connecting the different VLSI electronics by the Fresnel hologram is very similar to the fiber-optical interconnect. Therefore, we have the two following equations:

$$A_{Fresnel} = N_C(A_S + A_D) + A_{electronic}, \quad (34)$$

$$t_{fresnel} = t_S + t_D + t_{electronic}. \quad (35)$$

We summarize the comparison results for the area and latency of different optoelectronic interconnects in Table II.

Consider an example of a calculation comparing the three types of interconnects. We choose to use Finisar's VCSEL [56] as the single pixel's source. Its rise time and fall time are each 40 ps. The area occupied per source pixel is 0.250 mm^2. We use Alphalas' ultrafast photodetector [57] as the detector. Its response time ranges from 30 to 500 ps. We choose to use 50 ps as our calculation base and 0.250 mm^2 for the single detector's area. Assume the use of only four inputs for interconnection. Then the occupied area for both fiber-optical and Fresnel hologram interconnects is about 2.0 mm^2 plus the electronic component's size. At present, a 45 nm CMOS process for a complex bus switching logic should be less than 1.0 mm^2, so the total area is about 3.0 mm^2. For both fiber-optical and Fresnel hologram interconnects, the total latency will be 90 ps plus the electronic component's delay $t_{electronic}$. According to the International Technology Roadmap for Semiconductors (ITRS) [58], $t_{electronic}$ is about 0.7 ns (700 ps), $t_{electronic}$ may reduce to 0.2 ns (200 ps) by the year 2022. If we use 2 mW per VCSEL [56] and 1 mW per detector [57] for calculation, the total consumed power is approximately equal to 13 mW. However, for a 3-D free-space optoelectronic interconnect network, the total occupied area (one column only) is approximately equal to 10 mm^2+6 mm^2 ≅ 16 mm^2, the total latency will be 140 ps+6 ns (XOR gates), and the total consumed power will be approximately equal to 147.8 mW. However, if we use the optical MEMS interconnects, the latency will be in the 12 μs range. This is very slow compared with other types of interconnects. Note that this data is only a preliminary calculation, and the technology parameters vary from time to time.

TABLE II
COMPARISON OF AREA AND LATENCY OF DIFFERENT OPTOELECTRONIC INTERCONNECTS

Optoelectronic Interconnects	Area	Latency
Fiber-optical interconnect	$A_{OF}=N_C(A_S+A_D)+A_{electronic}$	$t_{OF}=t_S+t_D+t_{electronic}$
Fresnel hologram interconnect	$A_{fresnel}=N_C(A_S+A_D)+A_{electronic}$	$t_{fresnel}=t_S+t_D+t_{electronic}$
Free-space optoelectronic interconnect network	$V_{3D}=\frac{1}{2}(A_S+A_D)\times 4f$ $d_s=\frac{2.44\lambda f}{D}$ $A_s=[W_s+(2^{m+1}-1)d_s]\times[W_s+(2N-1)d_s]+A_{XOR}N$ $A_D=[W_D+(2n-1)d_D]\times[W_D+(2N-1)d_D]+(A_{cmps}+A_{adders})\times nN$	$t_{3D}=t_s+t_D+t_{XOR}+t_{cmps}+t_{adders}$
Optical MEMS interconnect	$W_{base}=A_s+4A_D+2A_{DMD}+6d$ $A_{MEM}=W_{base}l$	$t=t_s+t_D+2t_{DMD}$

VI. POWER CONSUMPTION COMPARISON

To compute the power consumption, assume that there are N_C interconnect points. The power required by the fiber-optical interconnect is then

$$P_{OF} = N_C(P_S + P_D) + P_{electronic}, \quad (36)$$

where P_S is the power required by a source, P_D is the power required by a detector, and $P_{electronic}$ is the power consumed by all electronic components.

The physical principle to connect the different VLSIs using the Fresnel hologram interconnect is very similar to the fiber optical interconnect method. Therefore, we have the following equation:

$$P_{Fresnel} = N_C(P_S + P_D) + P_{electronics}. \quad (37)$$

We summarize the comparison of the power consumptions of different optoelectronic interconnects in Table III. Symbols used are shown in Table IV.

VII. DISCUSSION AND CONCLUSION

Silicon photonic interconnects have received a lot of attention recently [59–65]. Miller [59] made a significant contribution to compare electrical and optical interconnects and examine the requirements for optoelectronic and optical devices for future silicon chips. Moreover, silicon photonic interconnects have been demonstrated successfully in intrachip clock distribution [62]. However, we have not discovered a revolutionary approach such that an entire VLSI chip can be replaced by optoelectronics [65]. New research may be required to study power loss and the optical bit error rate in silicon photonic interconnects.

In this paper, we derive and prove the algorithm to be used in a 3-D free-space optoelectronic interconnec-

TABLE III
COMPARISON OF POWER CONSUMPTIONS OF DIFFERENT OPTOELECTRONIC INTERCONNECTS

Optoelectronic Interconnects	Power Consumption
Fiber-optical interconnect	$P_{OF}=N_C(P_S+P_D)+P_{electronic}$
Fresnel hologram interconnect	$P_{Fresnel}=N_C(P_S+P_D)+P_{electronic}$
Free–space optoelectronic interconnect network	$P_{3D}=2^{m+2}\times NP_S+nN\times 4P_d+P_{XOR}+P_{cmps}+P_{adders}$ $\approx(2^{m+2}\times P_S+4nP_d)\times N$
Optical MEMS interconnect	$P=(P_S+2P_{DMD}+4P_D)l$

tion network. We introduce sophisticated mathematical equations for different types of optoelectronic interconnects. Among the four types of optoelectronic interconnects, according to our preliminary analysis, both the fiber-optical interconnects and the 3-D free-space optical interconnect network have the potential for future short-distance interconnection. Since the bus switching logic's signals are generated electronically, this may reduce the bit error propagation. In addition, the bus switching logics are inherently embedded inside the hologram. This can further reduce the size and consumed power, while at the same time increase the computational bandwidth. However, due to the bipolar encoding scheme, this technology has a larger power consumption and occupies a larger area than the traditional electronic interconnect.

TABLE IV
SYSTEM SYMBOLS USED IN THE CALCULATIONS

Nomenclature	Explanation
$t_{3\text{-}D}$	Total latency delay in 3-D optoelectronic interconnection network
t_{OF}	Total latency delay in fiber-optical interconnections
$t_{fresnel}$	Total latency delay in Fresnel hologram interconnect
t_s	Response time per source pixel (VCSEL or modulator)
t_d	Response time per detector
t_{DMD}	Response time per DMD device
λ	Optical wavelength
D	Lens diameter
N_C	Number of connection points for point-to-point interconnects
P_S	Power consumed per source pixel
P_D	Power consumed per detector
P_{DMD}	Power consumed per DMD pixel
A_S	Area occupied per source pixel
A_D	Area occupied per detector
A_{DMD}	Area occupied per DMD pixel
$A_{electronics}$	Total area occupied by electronics
$P_{electronics}$	Total power consumed by electronics
m	Number of input columns in truth table
n	Number of output columns in truth table

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